

WEST**Generate Collection****Print****Search Results - Record(s) 1 through 8 of 8 returned.** **1. Document ID: US 4860191 A**

L2: Entry 1 of 8

File: USPT

Aug 22, 1989

US-PAT-NO: 4860191

DOCUMENT-IDENTIFIER: US 4860191 A

TITLE: Coprocessor with dataflow circuitry controlling sequencing to execution unit of data received in tokens from master processor

L2: Entry 1 of 8

File: USPT

Aug 22, 1989

US-PAT-NO: 4860191

DOCUMENT-IDENTIFIER: US 4860191 A

TITLE: Coprocessor with dataflow circuitry controlling sequencing to execution unit of data received in tokens from master processor

DATE-ISSUED: August 22, 1989

INT-CL: [4] G06F 15/16, G06F 15/20, G06F 13/38

US-CL-ISSUED: 364/200

US-CL-CURRENT: 710/110; 712/201

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWMC
Draw Desc Image											

 2. Document ID: US 4811345 A

L2: Entry 2 of 8

File: USPT

Mar 7, 1989

US-PAT-NO: 4811345

DOCUMENT-IDENTIFIER: US 4811345 A

TITLE: Methods and apparatus for providing a user oriented microprocessor test interface for a complex, single chip, general purpose central processing unit

L2: Entry 2 of 8

File: USPT

Mar 7, 1989

US-PAT-NO: 4811345

DOCUMENT-IDENTIFIER: US 4811345 A

TITLE: Methods and apparatus for providing a user oriented microprocessor test interface for a complex, single chip, general purpose central processing unit

DATE-ISSUED: March 7, 1989

INT-CL: [4] G06F 11/00

US-CL-ISSUED: 371/16; 364/200

US-CL-CURRENT: 714/27

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/> <u>3631405</u>	December 1971	Hoff et al.	395/650
<input type="checkbox"/> <u>4276594</u>	June 1981	Morley	395/800
<input type="checkbox"/> <u>4541048</u>	September 1985	Propster et al.	395/375
<input type="checkbox"/> <u>4594651</u>	June 1986	Jaswa et al.	364/131
<input type="checkbox"/> <u>4641238</u>	February 1987	Kneib	395/290
<input type="checkbox"/> <u>4799144</u>	January 1989	Parruck et al.	364/200
<input type="checkbox"/> <u>4811345</u>	March 1989	Johnson	395/183.03
<input type="checkbox"/> <u>4860191</u>	August 1989	Nomura et al.	395/290
<input type="checkbox"/> <u>4862407</u>	August 1989	Fette et al.	395/800
<input type="checkbox"/> <u>4876660</u>	October 1989	Owen et al.	364/754
<input type="checkbox"/> <u>4908825</u>	March 1990	Vea	370/110.3
<input type="checkbox"/> <u>4975947</u>	December 1990	Chauvel	379/334
<input type="checkbox"/> <u>4991169</u>	February 1991	Davis et al.	370/77
<input type="checkbox"/> <u>5005168</u>	April 1991	Cummiskey et al.	370/24
<input type="checkbox"/> <u>5029204</u>	July 1991	Shenoi et al.	379/407
<input type="checkbox"/> <u>5036539</u>	July 1991	Wrench, Jr. et al.	395/2.55
<input type="checkbox"/> <u>5045993</u>	September 1991	Murakami et al.	395/375
<input type="checkbox"/> <u>5111530</u>	May 1992	Kutaragi et al.	395/2.79
<input type="checkbox"/> <u>5155852</u>	October 1992	Murakami et al.	395/725
<input type="checkbox"/> <u>5185599</u>	February 1993	Doornink et al.	395/143
<input type="checkbox"/> <u>5208832</u>	May 1993	Greiss	364/715.11
<input type="checkbox"/> <u>5293586</u>	March 1994	Yamazaki et al.	395/164

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
299537	January 1989	EPX	

OTHER PUBLICATIONS

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 "A Next-Generation 32 bit VLSI Signal Processor"; Shinjo Tsujimichi et al.; ICASSP 86, Tokio; 1986 IEEE; pp. 415-416.
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Precise Exceptions"; pp. 77-87; IEEE 1988.
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processing system": 5th International Conference on Systems Engineering: Fairborn,
Ohio, 9th-11th; Sep. 1987, pp. 447-450, IEEE, New York, US.
M.L. Fuccio et al: "The DSP32C: AT&T's second-generation floating-point digital signal
processor": IEEE Micro, vol. 8, No. 6, Dec. 1988, pp. 30-47, IEEE, New York, US.

ART-UNIT: 232

PRIMARY-EXAMINER: Pan; Daniel H.

ATTY-AGENT-FIRM: Limbach & Limbach L.L.P.

ABSTRACT:

An integrated data processing platform for processing a digital signal that includes a general purpose processor and a digital signal processor (DSP) module. The DSP module recovers digital data from a digital signal utilizing a sequence of DSP operations selected by the general purpose processor. The general purpose processor processes the digital data recovered by the DSP module, but is also available to perform general purpose tasks. A shared internal memory array selectively provides information to the DSP module and to the general purpose processor. The information stored in the internal memory array includes operands utilized in the execution of the DSP algorithm and selected instructions and data utilized by the general purpose CPU either for controlling the execution of the DSP algorithm or for executing its own general purpose tasks. While in many applications the data processing system will include an analog front end that converts a modulated input signal received on an analog transmission channel to a corresponding digital signal for processing by the data processing system, the data processing system may also receive the digital signal directly from a digital source.

10 Claims, 11 Drawing figures

FIELD-OF-SEARCH: 371/15, 371/16, 371/17, 371/18, 371/20, 324/73R, 324/73AT, 364/2MSFile

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc Image											

3. Document ID: US 4799144 A

L2: Entry 3 of 8

File: USPT

Jan 17, 1989

US-PAT-NO: 4799144

DOCUMENT-IDENTIFIER: US 4799144 A

TITLE: Multi-function communication board for expanding the versatility of a computer

L2: Entry 3 of 8

File: USPT

Jan 17, 1989

US-PAT-NO: 4799144

DOCUMENT-IDENTIFIER: US 4799144 A

TITLE: Multi-function communication board for expanding the versatility of a computer

DATE-ISSUED: January 17, 1989

INT-CL: [4] G06F 3/16

US-CL-ISSUED: 364/200; 379/284

US-CL-CURRENT: 710/2; 379/284, 379/387.01, 379/88.01, 379/88.07, 379/908, 704/275,
712/33, 712/38, 712/43

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile, 381/36-40, 340/825.19, 179/6.08, 179/6.06,
179/18BC, 179/18G, 379/88, 379/89, 379/96, 379/284, 379/97

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc Image											

4. Document ID: US 4641238 A

L2: Entry 4 of 8

File: USPT

Feb 3, 1987

US-PAT-NO: 4641238

DOCUMENT-IDENTIFIER: US 4641238 A

TITLE: Multiprocessor system employing dynamically programmable processing elements controlled by a master processor

L2: Entry 4 of 8

File: USPT

Feb 3, 1987

US-PAT-NO: 4641238

DOCUMENT-IDENTIFIER: US 4641238 A

TITLE: Multiprocessor system employing dynamically programmable processing elements controlled by a master processor

DATE-ISSUED: February 3, 1987

INT-CL: [4] G06F 15/16

US-CL-ISSUED: 364/200

US-CL-CURRENT: 710/110; 902/2, 902/39

FIELD-OF-SEARCH: 364/200, 364/900

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc Image					KWMC				

5. Document ID: US 4594651 A

L2: Entry 5 of 8

File: USPT

Jun 10, 1986

US-PAT-NO: 4594651

DOCUMENT-IDENTIFIER: US 4594651 A

TITLE: Concurrent processor for control

L2: Entry 5 of 8

File: USPT

Jun 10, 1986

US-PAT-NO: 4594651

DOCUMENT-IDENTIFIER: US 4594651 A

TITLE: Concurrent processor for control

DATE-ISSUED: June 10, 1986

INT-CL: [4] G06F 9/00

US-CL-ISSUED: 364/131; 364/180

US-CL-CURRENT: 700/2FIELD-OF-SEARCH: 364/131, 364/135, 364/2MSFile, 364/180, 364/160, 364/704, 318/590,
318/596

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc Image					KWMC				

6. Document ID: US 4541048 A

L2: Entry 6 of 8

File: USPT

Sep 10, 1985

US-PAT-NO: 4541048

DOCUMENT-IDENTIFIER: US 4541048 A

TITLE: Modular programmable signal processor

L2: Entry 6 of 8

File: USPT

Sep 10, 1985

US-PAT-NO: 4541048

DOCUMENT-IDENTIFIER: US 4541048 A

TITLE: Modular programmable signal processor

DATE-ISSUED: September 10, 1985

INT-CL: [3] G06F 7/38, G06F 15/00

US-CL-ISSUED: 364/200; 364/736

US-CL-CURRENT: 712/32; 708/524

FIELD-OF-SEARCH: 364/200, 364/736

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc Image					KMC				

7. Document ID: US 4276594 A

L2: Entry 7 of 8

File: USPT

Jun 30, 1981

US-PAT-NO: 4276594

DOCUMENT-IDENTIFIER: US 4276594 A

TITLE: Digital computer with multi-processor capability utilizing intelligent composite memory and input/output modules and method for performing the same

L2: Entry 7 of 8

File: USPT

Jun 30, 1981

US-PAT-NO: 4276594

DOCUMENT-IDENTIFIER: US 4276594 A

TITLE: Digital computer with multi-processor capability utilizing intelligent composite memory and input/output modules and method for performing the same

DATE-ISSUED: June 30, 1981

INT-CL: [3] G06F 15/16, G06F 13/00

US-CL-ISSUED: 364/200

US-CL-CURRENT: 713/600

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc Image					KMC				

8. Document ID: US 3631405 A

L2: Entry 8 of 8

File: USPT

Dec 28, 1971

US-PAT-NO: 3631405

DOCUMENT-IDENTIFIER: US 3631405 A

TITLE: SHARING OF MICROPROGRAMS BETWEEN PROCESSORS

L2: Entry 8 of 8

File: USPT

Dec 28, 1971

US-PAT-NO: 3631405

DOCUMENT-IDENTIFIER: US 3631405 A

TITLE: SHARING OF MICROPROGRAMS BETWEEN PROCESSORS

DATE-ISSUED: December 28, 1971

INT-CL: [] G06f 9/12, G06f 15/16

US-CL-ISSUED: 340/172.5

US-CL-CURRENT: 712/209, 709/310, 709/312, 712/226, 712/229, 712/246, 712/247

FIELD-OF-SEARCH: 340/172.5

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc Image					KMC				

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Term	Documents
"3631405".USPT.	1
3631405S	0
"4276594".USPT.	1
4276594S	0
"4541048".USPT.	1
4541048S	0
"4594651".USPT.	1
4594651S	0
"4641238".USPT.	1
4641238S	0
"4799144".USPT.	1
(3631405.PN. OR 4276594.PN. OR 4541048.PN. OR 4594651.PN. OR 4641238.PN. OR 4799144.PN. OR 4811345.PN. OR 4860191.PN.).USPT.	8

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1. Document ID: US 6175912 B1

L5: Entry 1 of 10

File: USPT

Jan 16, 2001

US-PAT-NO: 6175912

DOCUMENT-IDENTIFIER: US 6175912 B1

TITLE: Accumulator read port arbitration logic

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

2. Document ID: US 5911082 A

L5: Entry 2 of 10

File: USPT

Jun 8, 1999

US-PAT-NO: 5911082

DOCUMENT-IDENTIFIER: US 5911082 A

TITLE: Parallel processing building block chip

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

3. Document ID: US 5812562 A

L5: Entry 3 of 10

File: USPT

Sep 22, 1998

US-PAT-NO: 5812562

DOCUMENT-IDENTIFIER: US 5812562 A

TITLE: Low cost emulation scheme implemented via clock control using JTAG controller in a scan environment

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

4. Document ID: US 5727194 A

L5: Entry 4 of 10

File: USPT

Mar 10, 1998

US-PAT-NO: 5727194

DOCUMENT-IDENTIFIER: US 5727194 A

TITLE: Repeat-bit based, compact system and method for implementing zero-overhead loops

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc Image									KMC

 5. Document ID: US 5619514 A

L5: Entry 5 of 10

File: USPT

Apr 8, 1997

US-PAT-NO: 5619514

DOCUMENT-IDENTIFIER: US 5619514 A

TITLE: In-place present state/next state registers

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc Image									KMC

 6. Document ID: US 5559837 A

L5: Entry 6 of 10

File: USPT

Sep 24, 1996

US-PAT-NO: 5559837

DOCUMENT-IDENTIFIER: US 5559837 A

TITLE: Efficient utilization of present state/next state registers

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc Image									KMC

 7. Document ID: US 5465275 A

L5: Entry 7 of 10

File: USPT

Nov 7, 1995

US-PAT-NO: 5465275

DOCUMENT-IDENTIFIER: US 5465275 A

TITLE: Efficient utilization of present state/next state registers

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc Image									KMC

 8. Document ID: JP 62097062 A

L5: Entry 8 of 10

File: JPAB

May 6, 1987

PUB-NO: JP362097062A

DOCUMENT-IDENTIFIER: JP 62097062 A

TITLE: DIGITAL SIGNAL PROCESSOR

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc Image					KMC				

 9. Document ID: JP 10143364 A

L5: Entry 9 of 10

File: DWPI

May 29, 1998

DERWENT-ACC-NO: 1998-367366

DERWENT-WEEK: 199832

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TITLE: Digital signal processor - has processor core and user circuit on single chip by which un-registered user instruction and registered user instruction are decoded and executed

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc Clip Img Image					KMC				

 10. Document ID: CN 1174353 A, DE 19735348 A1, FR 2752965 A1, JP 10116268 A, US 5838984 A, TW 345650 A, KR 98018072 A, KR 236527 B1

L5: Entry 10 of 10

File: DWPI

Feb 25, 1998

DERWENT-ACC-NO: 1998-170237

DERWENT-WEEK: 200171

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TITLE: Digital signal parallel vector processor for multimedia applications - has single instruction multiple data processor using several banks of vector registers

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc Clip Img Image					KMC				

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Term	Documents
SINGLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1985971
SINGLES.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1792
INSTRUCTION\$	0
INSTRUCTION.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	208503
INSTRUCTIONA.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	26
INSTRUCTIONABLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
INSTRUCTIONADDRESS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2
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INSTRUCTIONAL.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	6780
(SINGLE NEAR4 INSTRUCTION\$ NEAR9 (DSP OR DIGITAL NEAR1 SIGNAL) NEAR10 REGISTER\$).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	10

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INSTRUCTIONS\$	0
INSTRUCTION.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	208503
INSTRUCTIONA.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	26
INSTRUCTIONABLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
INSTRUCTIONADDRESS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2
INSTRUCTIONADRESSER.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
INSTRUCTIONAI.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
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(SINGLE NEAR4 INSTRUCTIONS\$ NEAR9 (DSP OR DIGITAL NEAR1 SIGNAL) NEAR10 REGISTER\$).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	10

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DATE: Monday, February 25, 2002 [Printable Copy](#) [Create Case](#)

<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u>
side by side			result set

DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR

L5 single near4 instruction\$ near9 (dsp or digital near1 signal) near10
register\$

10 L5

L4 L3 and general near1 purpose

77 L4

L3 single near4 instruction\$ near9 (dsp or digital near1 signal)

160 L3

DB=USPT; PLUR=YES; OP=OR

L2 3631405.pn. or 4276594.pn. or 4541048.pn. or 4594651.pn. or
4641238.pn. or 4799144.pn. or 4811345.pn. or 4860191.pn.

8 L2

DB=EPAB; PLUR=YES; OP=OR

L1 299537

1 L1

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Search Results -

Term	Documents
SINGLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1985971
SINGLES.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1792
INSTRUCTIONS\$	0
INSTRUCTION.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	208503
INSTRUCTIONA.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	26
INSTRUCTIONABLE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
INSTRUCTIONADDRESS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2
INSTRUCTIONADRESSER.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
INSTRUCTIONAL.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
INSTRUCTIONAL.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	6780
INSTRUCTIONALLY.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	13
REGISTER\$(REGISTER-0-FLAG).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	pickup term
(SINGLE NEAR4 INSTRUCTION\$ NEAR9 (DSP OR DIGITAL NEAR1 SIGNAL) NEAR10 REGISTER\$).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	10

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- US Pre-Grant Publication Full-Text Database
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Search History

DATE: Monday, February 25, 2002 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR

L5 single near4 instruction\$ near9 (dsp or digital near1 signal) near10
register\$

10 L5

L4 L3 and general near1 purpose

77 L4

L3 single near4 instruction\$ near9 (dsp or digital near1 signal)

160 L3

DB=USPT; PLUR=YES; OP=OR

L2 3631405.pn. or 4276594.pn. or 4541048.pn. or 4594651.pn. or
4641238.pn. or 4799144.pn. or 4811345.pn. or 4860191.pn.

8 L2

DB=EPAB; PLUR=YES; OP=OR

L1 299537

1 L1

END OF SEARCH HISTORY

WEST**End of Result Set** [Generate Collection](#) [Print](#)

L1: Entry 1 of 1

File: USPT

May 13, 1997

US-PAT-NO: 5630153

DOCUMENT-IDENTIFIER: US 5630153 A

TITLE: Integrated digital signal processor/general purpose CPU with shared internal memory

DATE-ISSUED: May 13, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Intrater; Amos	Lantau			HKX
Doron; Moshe	Sunnyvale	CA		
Intrater; Gideon	Ramat-Gan			ILX
Epstein; Lev	Holon			ILX
Valentaten; Maurice	Geldtendorf			DEX
Greiss; Israel	Raanana			ILX

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
National Semiconductor Corporation	Santa Clara	CA			02

APPL-NO: 8 / 317783 [PALM]

DATE FILED: October 4, 1994

PARENT-CASE:

This is a continuation of application Ser. No. 08/011,102 filed on Jan. 29, 1993, now abandoned, which is a continuation of application Ser. No. 07/467,148 filed on Jan. 18, 1990 now abandoned.

INT-CL: [6] G06 F 9/26, G06 F 9/40, G06 F 9/44, G06 F 13/36

US-CL-ISSUED: 395/800, 395/290, 395/306, 364/DIG.1, 364/DIG.2

US-CL-CURRENT: 712/35; 710/110, 712/36

FIELD-OF-SEARCH: 395/800, 395/290, 395/200.01, 395/375, 395/200.03, 395/700, 395/289, 395/287, 395/297, 395/2.79, 395/183.19, 395/2.55, 395/775, 395/306, 364/DIG.1, 364/DIG.2, 364/706, 364/736, 364/726

PRIOR-ART-DISCLOSED:

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L1: Entry 1 of 1

File: EPAB

Jan 18, 1989

PUB-NO: EP000299537A2

DOCUMENT-IDENTIFIER: EP 299537 A2

TITLE: Apparatus and Method for processing digital signal.

PUBN-DATE: January 18, 1989

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INT-CL (IPC): G06F 15/00

EUR-CL (EPC): G06F015/78; G06F017/10

ABSTRACT:

CHG DATE=19990617 STATUS=O> An apparatus for processing a digital signal includes a pair of data buses (11), a pair of digital processing circuits (12, 13) respectively connected to corresponding one of the data buses, and a control circuit (20) which simultaneously controls the digital processing circuits. To the digital processing circuits, an external storage including cyclic storage areas is connected. The digital processing circuits evaluate an actual address data for the cyclic storage areas of the external storage by means of predetermined arithmetic operation. The actual address data is outputted through the data buses and an external storage interface circuit (16) to the external storage. An address data being stored in a storage of the digital processing circuit is read. During one instruction cycle, the read address data is incremented or decremented, and when the result thereof is a boundary of the cyclic storage areas, a predetermined value is outputted from an ALU (28). A starting address is added to the predetermined value and a result thereof is outputted as the actual address data.